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DEVELOPMENT OF A Ge/GaAs HMT TECHNOLOGY BASED ON PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION

Quarterly Report -- Third Quarter

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The following report details the progress on ONR contract number N-00014-86-C-0838 during the period from 1 July 1989 to 30 September 1989. This program is targeted at development of a Ge on GaAs High Mobility Transistor (HMT) technology. Work during this quarter has focused on development of the n channel MISFET fabrication process. This quarterly report discusses the results of the selectively implanted source drain FETs.

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1.0 INTRODUCTION

The following report details the progress on ONR contract number N00014-86-C-0838 during the period from 1 July 1989 to 30 September 1989. Funding is being provided by the Strategic Defense Initiative under the Innovative Science and Technology division through the Office of Naval Research. This program is targeted at development of a Ge on GaAs High Mobility Transistor (HMT) technology.

Work during this quarter has focused on development of the n channel MIS-FET fabrication process. Two different FET processes have been implemented. One process uses a blanket implant and etched source drain mesas. The other process uses selectively implanted source and drain regions. In the case of the blanket implanted wafer, we have found that annomolous diffision of the implanted phosphorus led to difficulty in isolating the source drain regions. The use of the selective implant process has solved the isolation problem. The results of the etched mesa FETs were described in the previous quarterly reports. This quarterly report discusses the results of the selectively implanted source drain FETs.

2.0 SELECTIVELY IMPLANTED Ge MISFET PROCESSING

Selective implantation of source and drain regions is the preferred technology for transistor fabrication over etched mesa source drain devices. This is particularly true in Ge where anomolous diffusion of implanted species has been found to occur. Proper processing of selectively implanted FET structures has allowed fabrication of inversion mode devices which can be turned off and which show reasonable device scaling performance.

The selectively implanted source drain regions were fabricated as outlined below:

2.1 Wafer Masking Procedure for Implantation

1. Solvent clean wafer in ultrasonic TCE, Acetone and Methanol.
2. Rinse wafer 5 minutes in running DI water.
3. Dry wafer on hotplate for 5 minutes at 90 ° C.
4. Spin on photoresist at 4000 RPM.
5. Soft bake for 1 minute on hot plate at 90 ° C.
6. Expose using 1 S/D (dark field) mask.
7. Develop using 1 to 5 developer to water.
8. Rinse in water for 10 minutes. Blow dry, and HARD BAKE.
9. Etch wafer in H2O2 solution 3 minutes.

   1:H2O2 10:H2O

10. Rinse in water 5 min. then blow dry.
11. Inspect wafer and package for shipping.

The hard bake process in step 8 is essential to avoid cracking of the photo resist during the implantation process.

The device fabrication process is completed as follows:

2.2 Ion Implantation Schedule

material-- Ge wafers p type (2 bare wafers)

implant species-- Phosphorus

double implant dose-energy schedule

1×10^{14} cm^{-2} at 100 KeV

1×10^{15} cm^{-2} at 50 KeV

2.3 Gate and Contact Formation

1. Deposit Si-SiO_2 gate insulator structure on wafer.
2. Sputter deposit 15 min of Al on front side of wafer and 5 min on backside.
3. Anneal wafer 30 min at 400 °C.
4. Spin on photoresist at 6000 rpm. Soft bake 1 min on 90 °C hotplate.
5. Align and expose the wafer using 3 Gate (light field) mask.
6. Develop, rinse, blow dry and hard bake the wafer.
7. Etch the aluminum using Transene etchant A.
8. Remove photoresist with acetone, rinse in acetone, methanol, water, blow dry.
9. Dry wafer 1 minute on hot plate.
10. Spin on photoresist at 6000 rpm. Soft bake 1 min on 90 °C hot plate.
11. Align and expose the wafer using 4 Contact (dark field) mask.
12. Develop, no hard bake. Etch 20 seconds in buffer HF, 1 min water rinse, blow dry.

13. Sputter deposit 5 min of Al on wafer.

14. Liftoff in acetone, rinse in fresh acetone, methanol, and water, blow dry.

15. Samples ready for testing.

The annealing of the implanted P takes place during the 400/(deC post metalization anneal process in step 3 of the contact process.

3.0 Ge MISFET ELECTRICAL PERFORMANCE

The MISFET devices described in this section are inversion mode n channel devices. The wafer was masked for implantation such that half of the wafer was completely covered to avoid any implantation, in order to evaluate the effect of the implantation. It was found that the implantation process had virtually no effect on the interface state density of the Ge-pseudomorphic Si-SiO_2 insulator structure.

Capacitance voltage characteristics of the implanted and unimplanted areas are shown in Figure 1. The interface state densities calculated from the CV data is in the low $10^{11}cm^{-2}ev^{-1}$ range for both samples. These devices have an oxide thickness of 13 nm. The p type CV characteristics bear out the fact that these are truly inversion mode devices. Previously reported devices had shown degraded n type CV behavior most likely due to annomolous diffusion of implanted species. Transistor characteristics are shown in Figure 2 for a 2 micron long device and in Figure 3 for a 4 micron long device. The threshold voltage for the devices is approximately -0.2 volts (from the CV characteristic). The maximum transconductance for the 2 micron device is 22 mS/mm and for the 4 micron device is

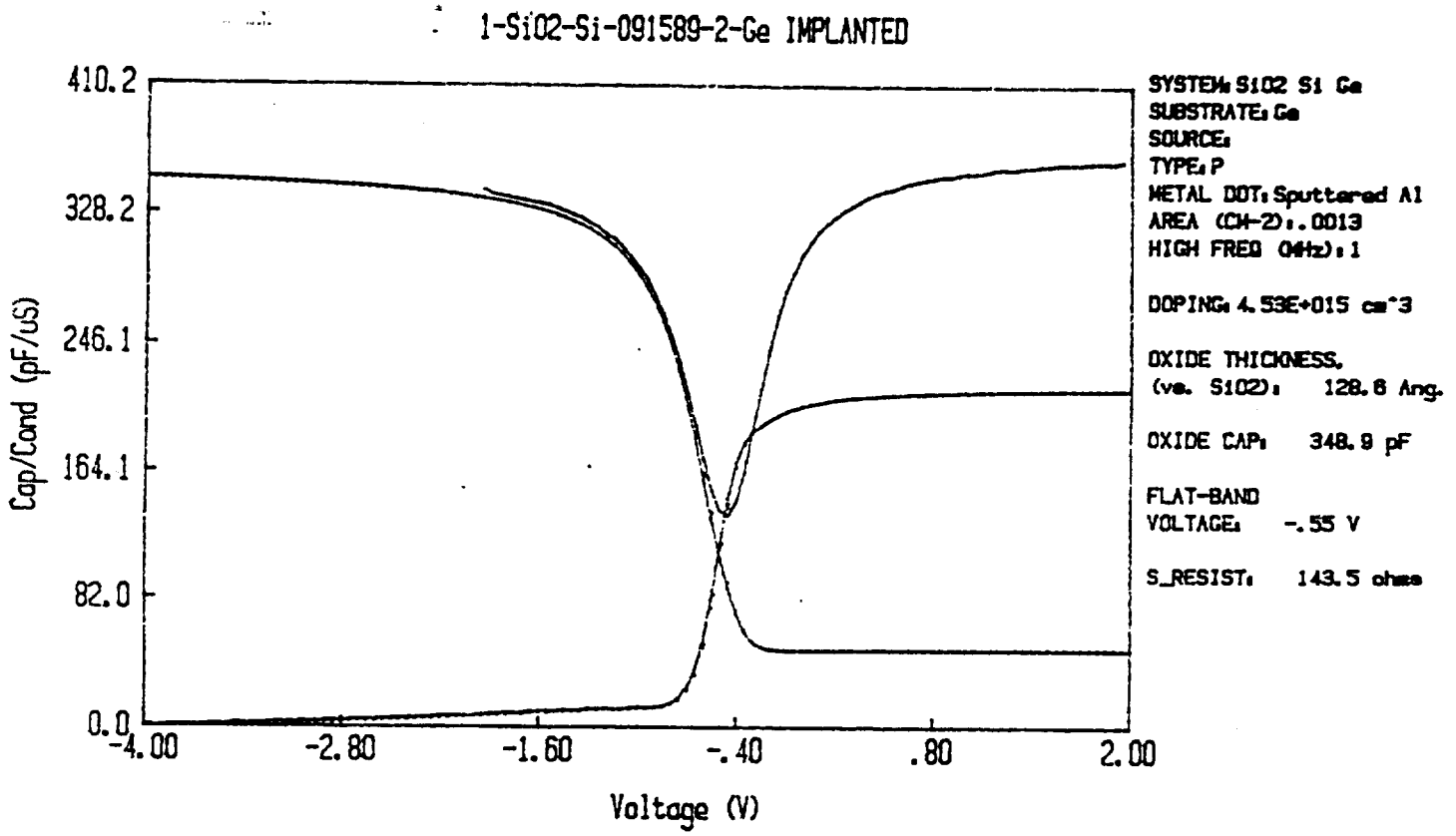

FIGURE 1a: Capacitance voltage characterstic of the active area of a test die which has been ion implanted in the source drain contact regions.

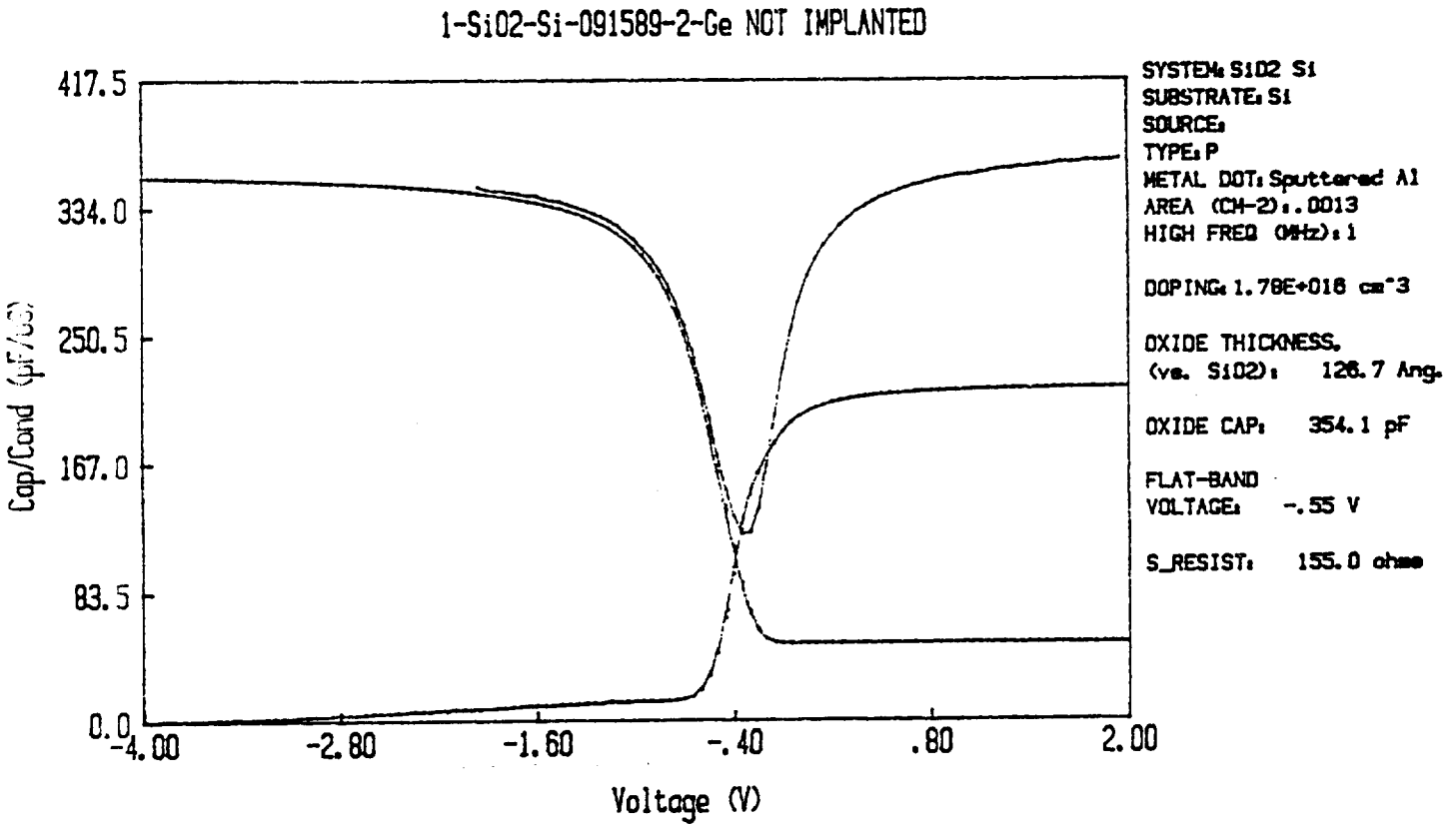

FIGURE 1b: Capacitance voltage characterstic of the active area of a test die which has not been ion implanted.

SAMPLE ID	: 1-S102-S1-091589-2-G	TEST DATE	: 10/04/89
FILE NAME	: 1G091589.2_4	RAMP RATE	: 1.0 V/S
GATE WIDTH	: 5.00E-2 mm	# GATE STEPS	: 6.00
GATE LENGTH	: 2.00E-3 mm	GATE START	: 0 Volts
GM (MAX)	: 2.24E1 mS/mm	GATE STEP	: 1 Volts

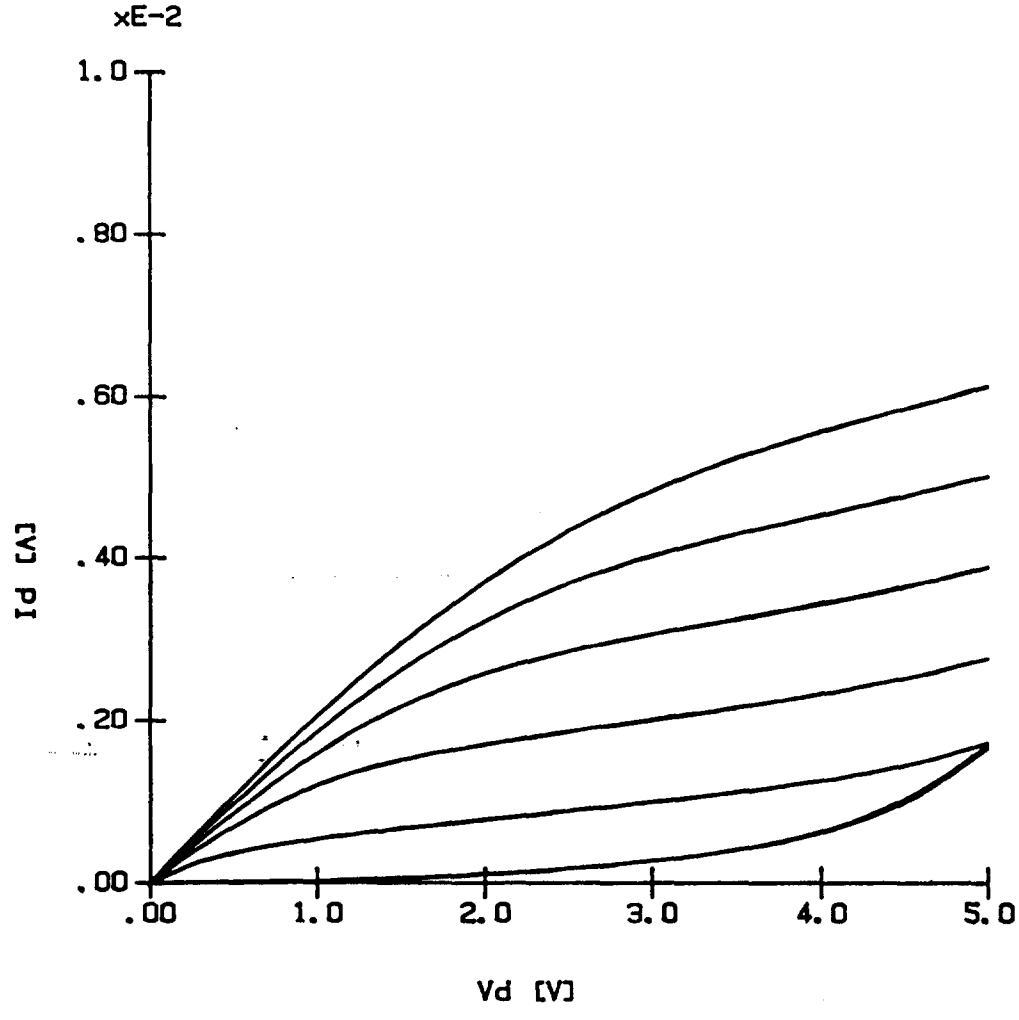

FIGURE 2: Transistor characteristics of a 2-micron inversion mode channel in Ge MISFET.

SAMPLE ID	: 1-S102-Si-091589-2-G	TEST DATE	: 10/04/89
FILE NAME	: 1G091589.2_B	RAMP RATE	: 1.0 V/S
GATE WIDTH	: 5.00E-2 mm	# GATE STEPS	: 6.00
GATE LENGTH	: 4.00E-3 mm	GATE START	: 0 Volts
GM (MAX)	: 1.42E1 mS/mm	GATE STEP	: 1 Volts

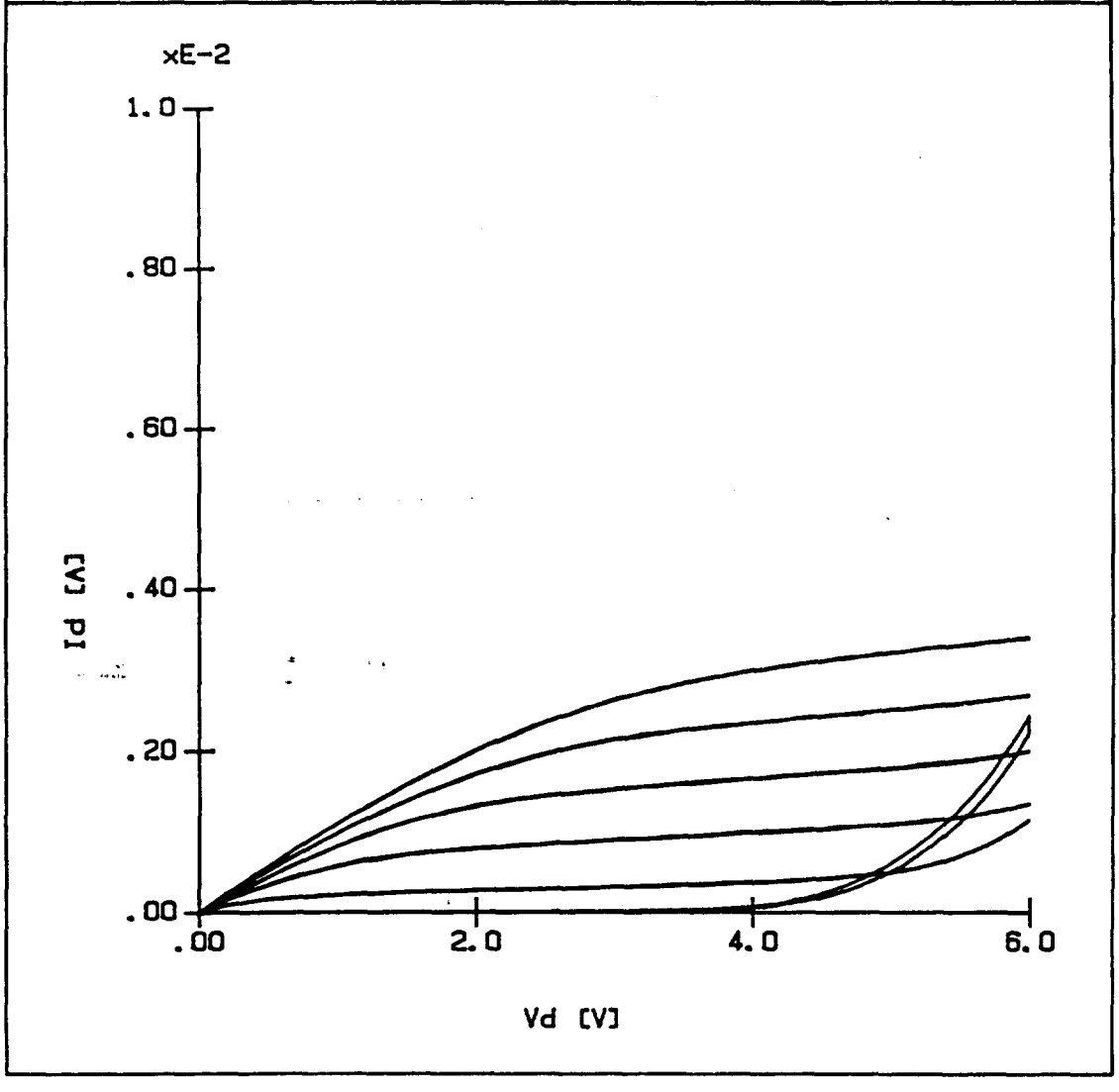

FIGURE 3: Transistor characteristics of a 4-micron inversion mode in channel Ge MISFET

14 mS/mm. There is no looping in the device characteristics. The leakage current of the turned off device is caused partially by the large area source drain regions (these regions were made large to facilitate probing).

4.0 SUMMARY AND PREVIEW

During the 3rd quarter Ge MISFET devices were fabricated using a selective implant technology for the source drain formation. The devices exhibited good transistor behavior with threshold voltages of about -0.2 volts and gains of 22 mS/mm at a gate length of 2 microns.

During the up coming quarter the channel mobility will be measured using the gated Hall pattern on the test die. Contact resistance values will also be measured.

In addition, TEM data of the Ge on GaAs epitaxy will be available for the annual report.